What is claimed is:

1. A dynamic circuit having an evaluation phase, the dynamic circuit comprising:

a node;

at least one nMOSFETs to conditionally pull the node LOW during the evaluation phase; and

a conditional keeper comprising

a NAND gate having a first input port connected to the node and an output port; and

a first pMOSFET having a gate connected to the output port of the NAND gate and having a drain connected to the node.

2. The dynamic circuit as set forth in claim 2, further comprising:

an inverter having an input port and an output port; and

a second pMOSFET having a gate connected to the output port of the inverter and having a drain connected to the node;

wherein the first pMOSFET is sized larger than the second pMOSFET.

3. The dynamic circuit as set forth in claim 2, the NAND gate further comprising:

a second input port, wherein the conditional keeper provides a keeper function for the node only if the second input port of the NAND gate is held HIGH.

4. The dynamic circuit as set forth in claim 1, the NAND gate further comprising:

a second input port, wherein the conditional keeper provides a keeper function for the node only if the second input port of the NAND gate is held HIGH.

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5. A dynamic circuit comprising:

a node having a voltage;

a pullup transistor to pull the node HIGH;

a network comprising at least one transistors to conditionally pull the node LOW if the pullup transistor is OFF;

a NAND gate having a first input port responsive to the node voltage, having an output port with a voltage, and having a second input port; and

a first transistor responsive to the output port voltage of the NAND gate to pull the node HIGH only if the second input port of the NAND gate is HIGH.

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6. The dynamic circuit as set forth in claim 5, further comprising:

an inverter coupled to the node; and

a second transistor coupled to the inverter and the node to provide a keeper function.

7. The dynamic circuit as set forth in claim 6, wherein the first transistor is sized larger than the second transistor.

8. A dynamic circuit having a normal operating condition and a burn-in condition, the dynamic circuit comprising:

a node having a voltage;

a network comprising at least one transistor to conditionally pull the node LOW;

a logic gate having a first input port responsive to the node voltage, a second input port, and an output port having a voltage;

a first transistor responsive to the output port voltage of the logic gate, and coupled to the node; and

wherein the first transistor and the logic gate provide a keeper function to the node if and only if the second input port of the logic gate is at a voltage indicative of the dynamic circuit being in the burn-in condition.

9. The dynamic circuit as set forth in claim 8, wherein the first transistor is a pMOSFET having a gate connected to the output port of the logic gate and a drain connected to the node.

10. The dynamic circuit as set forth in claim 9, wherein the logic gate is a NAND gate.

11. The dynamic circuit as set forth in claim 10, further comprising:

a second transistor to the node; and

an inverter coupled to the second transistor and the node, so that the combination of the second transistor and the inverter provide a keeper function to the node.

12. The dynamic circuit as set forth in claim 11, wherein the first transistor is sized larger than the second transistor.

13. The dynamic circuit as set forth in claim 8, further comprising:

a second transistor to the node; and

an inverter coupled to the second transistor and the node, so that the combination of the second transistor and the inverter provide a keeper function to the node.

14. The dynamic circuit as set forth in claim 13, wherein the first transistor is sized larger than the second transistor.